ABSTRACT OF THE DISCLOSURE

A delay circuit does not lead to excessive increase in the delay time even if the source voltage drops, and enables to control the delay time from increasing. The delay circuit is designed to delay a logic signal SIN having two logic levels consisting of a low level and a high level, such that the delay times are different for the high and low levels, and the circuit chooses either the low level or the high level and targets a logic level having a shorter delay time. That is, n-MOS transistors N11, N12 and p-MOS transistors P11, P12 are provided as MOS capacitors, so as to change from the off-state to the on-state during the transition period of a signal that appears on each node disposed on a delay path of logic signals. Such a circuit design enables to control source-voltage dependence of delay time so that, even if the source voltage drops, delay times are not increased excessively.